## IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An over-programming condition detector for use with an array of multistate memory cells, each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states, the detector comprising:

a first logic gate for detecting a first one of the at least four sequential data states in data intended to be written to the array;

a second logic gate for detecting a second one of the at least four sequential data states in data intended to be written to the array;

a third logic gate for detecting a third one of the at least four sequential data states in data intended to be written to the array; ~~and~~

a fourth logic gate for receiving data written to the array; and

over-programming detection logic connected to the first, second, third and fourth logic gates for generating an over-programming error signal.

2. (Currently Amended) The detector of claim 1, wherein ~~each~~ the first, second and third logic gate~~s~~ ~~is~~ are ~~an~~ AND gate~~s~~.

3. (Currently Amended) An over-programming condition detector for use with an array of multistate memory cells, each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states, the detector comprising:

a first logic gate for detecting a first one of the at least four sequential data states in data intended to be written to the array;

a second logic gate for detecting a second one of the at least four sequential data states in data intended to be written to the array;

a third logic gate for detecting a third one of the at least four sequential data states in data intended to be written to the array;

a fourth logic gate coupled to the ~~buffer~~ array and an output of the first logic gate for detecting a first over-programmed condition;

a fifth logic gate coupled to the ~~buffer~~ array and an output of the second logic gate for detecting a second over-programmed condition; and

a sixth logic gate coupled to the ~~buffer~~ array and an output of the third logic gate for detecting a third over-programmed condition.

4. (Original) The detector of claim 3, wherein each logic gate is an AND gate.

5. (Original) The detector of claim 3, further comprising a seventh logic gate coupled to respective outputs of the fourth, fifth, and sixth logic gates.

6. (Currently Amended) An over-programming condition detector for use with an array of multistate memory cells, each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states, the detector comprising:

a first logic gate for detecting a first one of the at least four sequential data states in data intended to be written to the array;

a second logic gate for detecting a second one of the at least four sequential data states in data intended to be written to the array;

a third logic gate for detecting a third one of the at least four sequential data states in data intended to be written to the array;

a fourth logic gate coupled to the ~~buffer~~ array, an enable input, and an output of the first logic gate for detecting a first over-programmed condition;

a fifth logic gate coupled to the ~~buffer~~ array, the enable input, and an output of the second logic gate for detecting a second over-programmed condition; and

a sixth logic gate coupled to the ~~buffer~~ array, the enable input, and an output of the third logic gate for detecting a third over-programmed condition.

7. (Original) The detector of claim 6, wherein each logic gate is an AND gate.

8. (Original) The detector of claim 6, further comprising a seventh logic gate coupled to respective outputs of the fourth, fifth, and sixth logic gates.

9. (Currently Amended) A multistate memory system comprising:

an array of multistate memory cells, with each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states;

a buffer for coupling to the array of multistate memory cells;

a memory programming module coupled to the buffer for programming each of the multistate memory cells to a desired one of the at least four sequential data states; and

at least one over-programming condition detector coupled to the memory programming module for generating an over-programmed signal representative of one or more of the memory cells having been erroneously programmed to one of the at least four sequential data states which is subsequent to the desired one of the at least four sequential data states, wherein the over-programming condition detector comprises:

a first logic gate for detecting a first one of the at least four sequential data states;

a second logic gate for detecting a second one of the at least four sequential data states;

a third logic gate for detecting a third one of the at least four sequential data states; ~~and~~

a fourth logic gate coupled to the buffer; and

over-programming detection logic connected to the first, second, third and fourth logic gates for generating an over-programming error signal.

10. (Currently Amended) The system of claim 9, wherein the memory programming module is configured to program each of the multistate memory cells to ~~a~~ the desired state of the at least four sequential data states.

11. (Original) The system of claim 9, wherein the memory programming module is configured to program multistate flash memory cells.

12. (Currently Amended) The system of claim 9, wherein ~~each~~ the first, second and third logic gates ~~is~~ are ~~an~~ AND gates.

13. (New) The detector of claim 1, wherein the fourth logic gate is a NAND gate.

14. (New) The detector of claim 1, wherein the over-programming detection logic includes a fifth gate for generating the over-programming error signal.

15. (New) The detector of claim 14, wherein the fifth gate is an OR gate.

16. (New) The detector of claim 5, wherein the seventh gate is an OR gate.

17. (New) The detector of claim 8, wherein the seventh gate is an OR gate.

18. (New) The system of claim 9, wherein the over-programming detection logic includes a fifth gate for generating the over-programming error signal.

19. (New) The system of claim 9, further comprising a controller connected to the memory programming module for controlling the memory programming module.

20. (New) The system of claim 19, further comprising static random access memory (SRAM) connected to the controller for storing code of one or more programs for execution using the controller.